A SINGLE CHIP C - BAND GaAs MONOLITHIC FIVE BIT PHASE SHIFTER WITH ON CHIP DIGITAL DECODER

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ABSTRACT

A single chip C-band GaAs monolithic five bit phase shifter with on-chip digital decode circuitry measuring 96mils x 48mils has been developed. This phase shifter has an RMS phase error of less than five degrees across 5.5-8.5 GHz band with greater than 60% RF yield. An application of this phase shifter as a serrodyne frequency translator is also presented.

INTRODUCTION

Recent publications have discussed a number of GaAs monolithic C-band phase shifter developments and show encouraging results for phased array applications. A 5-6 GHz six-bit phase shifter with conventional loaded transmission lines and reflection type design (4.19mm x 9.3mm) has been built [1]. A two-bit S-C band phase shifter using a novel switched filter approach incorporated the FETs as part of the filter networks [2] and measured 4.8 mm x 1.7 mm. An L-, S-, and C-band digitally controlled 0^{O}-90^{O} segmented dual gate FET vector modulator phase shifter [3] can be integrated with external 90^{O} hybrid, $0^{O}/180^{O}$ phase splitter and a combiner to achieve 0^{O}-360^{O} five bit performance. Another C-band (5-6 GHz) six bit switched filter phase shifter [4] was developed measuring 5.4 mm x 2.15 mm. A recently reported multifunction MMIC utilizes a S-C band six-bit switched filter phase shifter [5]. Some of these reported techniques consume large amount of GaAs real estate, and do not provide any on-chip decoding of control signals.

The C-band five-bit monolithic digital phase shifter reported here has been designed and fabricated with an emphasis on small chip size (96 mils x 48 mils), high yield (>60%), manufacturability and on-chip digital decoding.

MONOLITHIC PHASE SHIFTER: DEVELOPMENT AND OPERATION

Figure 1 shows a simplified block diagram of the five bit digital phase shifter consisting of baluns, quadrant select circuits, variable attenuators, passive in-phase combiners, and 90^{O} phase shift networks.

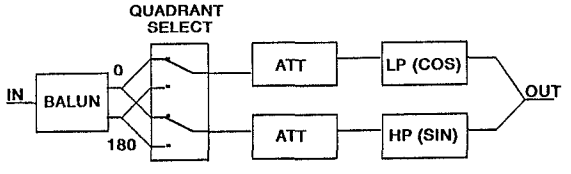

Figure 1. Block diagram of the five bit digital phase shifter

The C-band monolithic five bit phase shifter is implemented with a switched quadrant vector modulator approach. The phase shifter is required to shift insertion phase (<S21) from 0^{O} to 360^{O} in discrete steps, while maintaining constant magnitude. The 5-bit phase shifter developed here divides 360^{O} into 2^{5} or 32 increments, each of 11.25^{O}. The vector modulator operates within each quadrant by the vector addition of two signals 90^{O} out of phase, whose magnitudes are varied according to the sines and cosines of the desired phase shift.

The 90^{O} phase shift for the vector modulator is implemented with lumped element high-pass/low-pass filter networks, to provide a differential phase shift of 90^{O} in the desired band. The capacitors in the filters are realized using varactor diodes to allow voltage control of the capacitance value [6].

The variable attenuator used in the vector modulator consists of a set of parallel-connected dual gate FETs, biased as common source amplifiers. The RF signal is applied to the first gates, whose bias voltages are constant for all phase states. The

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voltages on the second gates switch the gain of each FET segment on or off.

An off-chip balun generates two signals 180° out of phase and switching between them allows phase shifts in all four quadrants. In addition to providing the 180° phase split, this technique eliminates the need for critical RF grounding with viaholes and allows a high level of integration in a small chip size.

The quadrant switching is accomplished with the same 90° differential phase shift networks that are used for the vector modulator. The 0° and 180° signals are each applied to a variable attenuator whose outputs are connected to the low pass network, for the cosine function of the vector modulator. The 90° and 270° (which are still 0o and 180o at the quadrant select point, but will be shifted 90o later) signals are applied to an attenuator with the high pass network, for the sine function. If the desired phase shift is 236.25°, the 180° signal is switched to the low pass network and attenuated by the cosine of 56.25°, and the 270° signal is switched to the high pass and attenuated by the sine of 56.25°.

DIGITAL DECODER CIRCUIT

The five-bit digital input is decoded on-chip to produce the 20 control signals for the variable attenuators. The logic was implemented with buffered FET logic standard cells using 1 um depletion mode FETs to ensure compatibility with the analog FET circuitry. The relative widths of the dual gate FETs in the variable attenuators were selected to minimize the decode circuitry. The digital decoder operates from +5V and -5V supplies and draws 50 mA.

A photograph of the fabricated five-bit phase shifter chip is shown in Figure 2. The chip measures only 96 mils x 48 mils. The bonding pads on the chip are four mil squares.

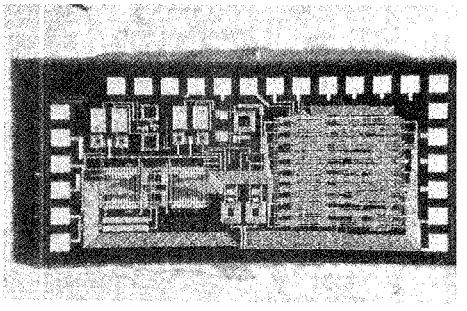

Figure 2. Photograph of the fabricated five-bit phase shifter with on-chip digital decoder

MEASURED PERFORMANCE OF THE DIGITAL PHASE SHIFTER

The phase shifter IC has been evaluated both at the wafer level and in a package. Wafer level measurements were performed using multicontact RF probes and a DC probe card (for feeding the digital control voltages). Figure 3 shows the phase performance of the phase shifter for all 32 phase states over 5.5 - 8.5 GHz frequency. The RMS phase error for a given frequency in the band and over the frequency band is less than 5 degrees. The insertion loss variation over all 32 phase states is -13 ±1 dB (Figure 4). The input and output VSWR of this phase shifter is better than 2:1. Sample test of phase shifters from several wafers have shown an RF yield of greater than 60%.

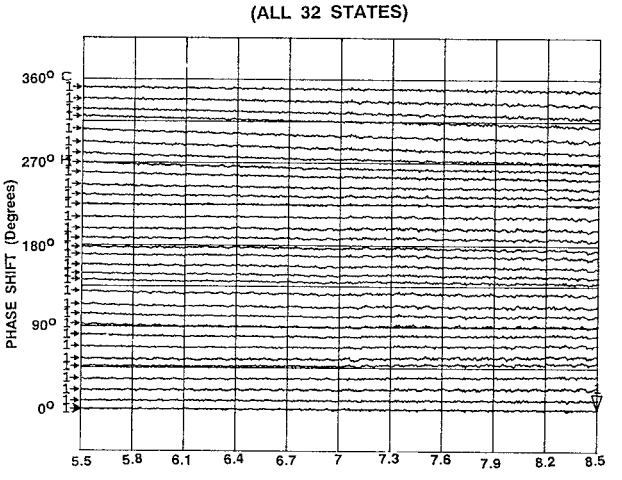

Figure 3. Five-bit phase shift performance of the digital phase shifter

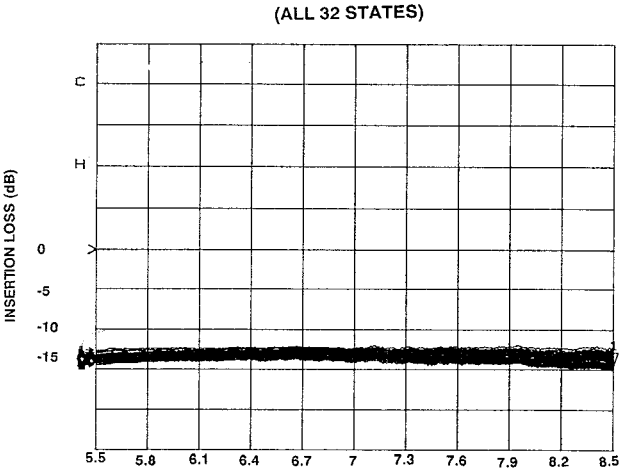

Figure 4. Insertion loss of the five-bit digital phase shifter

A photograph of the packaged phase shifter with input and output baluns and SMA connectors is shown in Figure 5.

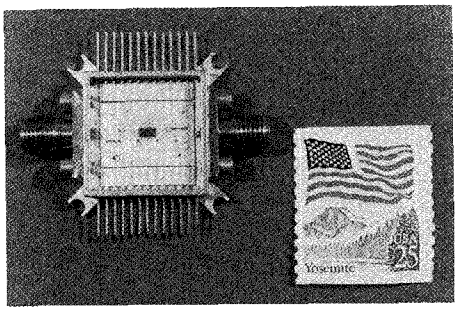

Figure 5. Photograph of the packaged phase shifter

APPLICATIONS

This monolithic phase shifter is appropriate for C-band phased array application where small die size is important for eventual cost effective T/R module production. It also finds application in serrodyne modulation, where this phase shifter can be combined with a monolithic clock driver circuit (Figure 6) in a package to simulate a Doppler shift [7]. Results of a packaged serrodyne modulator (Figure 7) at 7 GHz shows 22 dB of spur suppression.

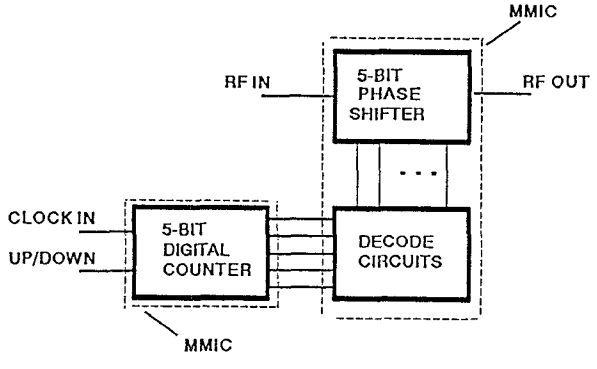

Figure 6. Application of the digital phase shifter as a serrodyne modulator

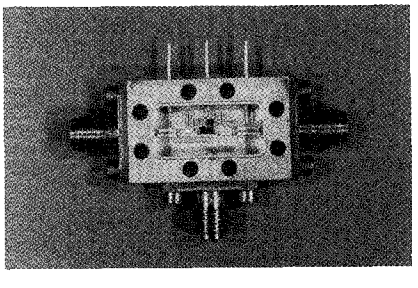

Figure 7. Photograph of a packaged serrodyne modulator

CONCLUSIONS

A C-band GaAs monolithic five-bit phase shifter with on-chip digital decoder has been developed. Small die size (96 mils x 48 mils), low phase error (RMS phase error $<5^{O}$) and high yield (>60%) will provide for low cost phase shifter manufacturability.

ACKNOWLEDGEMENT

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